WHAT IS CLAIMED:

1. A solid-state oscillator comprising an odd number of solid-state inverter devices cascaded in series, each inverter having an input and an output, the output of the last inverter being fed back to the input of the first inverter.

2. In combination with the oscillator of claim , a source of a clock signal;

a phase comparator receiving the clock signal as a first input and the input of the first inverter as a second input; the phase comparator producing a difference signal related to the phase difference between its inputs;

a voltage generator producing an output voltage and having a control input, the amplitude of the output voltage signal being controlled by a signal applied to the control input, the difference signal being applied to the control input;

the inverters having a reference voltage connection, the delay of an inverter being controlled by the value of the voltage applied to the reference voltage connection, the output voltage being applied to reference voltage connection; and

a combining circuit combining the outputs of N inverters;

the output of the combining circuit being at a frequency which is N times the clock frequency.

3. In combination with the combination of claim 2:

M solid state inverter devices cascaded in series to define a delay line, each inverter of the delay line having an input and an output, each inverter having a reference voltage connection, the delay of an inverter being controlled by the value of the voltage applied to the reference voltage connection, the output voltage being applied to reference voltage connections of the inverters;

a data signal being applied to the input of the first inventor of the delay line;

an M position latch receiving the outputs of the inverters of the delay line, the latch being clocked with the output of the combining circuit;

whereby M samples of the data signal are produced at a frequency which is N times the clock frequency.